distance between the shield layer and the drain extension region increases in a direction from the gate electrode towards the drain contact region.

2. A MOS transistor as claimed in claim **1**, wherein the shield layer comprises a multiple of portions extending over the drain extension region essentially parallel to a top surface of the drain extension region, in which a second distance between the drain extension region and a second portion of the shield layer is larger than a first distance between the drain extension region and a first portion of the shield layer, which first portion is closer to the gate electrode than the second portion of the shield layer.

3. A MOS transistor as claimed in claim **1**, wherein the shield layer comprises a multiple of stacked shield sub-layers, in which a second shield sub-layer extends over a first shield sub-layer and is separated from the first shield sub-layer by an isolation layer, and in which the second shield sub-layer extends over a larger part of the drain extension region than the first shield sub-layer, and in which a second distance between the second shield sub-layer and the drain extension region is larger than a first distance between the first shield sub-layer and the drain extension region.

4. A MOS transistor as claimed in claim **1**, wherein the shield layer also extends over a part of the gate electrode.

5. A MOS transistor as claimed in claim **4**, wherein the shield layer also extends over a part of the source region.

6. A MOS transistor as claimed in claim **5**, the MOS transistor further comprising a substrate contact region, which is adjacent to the source region, wherein the substrate contact region and the source region are electrically connected via a first interconnect layer.

7. A MOS transistor as claimed in claim **1**, wherein the shield layer is electrically connected to the source region.

8. A method of manufacturing the MOS transistor as claimed in claim **1**, comprising the step of providing a semiconductor substrate region in which a source region, a channel region, a drain extension region and a drain contact region are provided, wherein the drain extension region mutually connects the drain contact region and the channel region, and wherein the channel region mutually connects the drain extension region and the source region, the method further comprising the steps of:

forming a gate oxide layer on the semiconductor substrate region,

forming a gate electrode, extending over the channel region, on a first portion of the gate oxide layer,

forming an isolation region on a third portion of the gate oxide layer and extending over a part of the drain extension region, the third portion of the gate oxide layer being separated from the first portion of the gate oxide layer by a second portion of the gate oxide layer, and wherein the isolation region has a thickness that increases in a direction from the gate electrode towards the drain contact region, and

forming a shield layer of an electrically conductive material extending at least over a part of the second portion of the gate oxide layer and at least over a part of the isolation region.

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